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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,004	11/07/2001	Takuji Matsumoto	215544US2	4595

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EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/986,004	Applicant(s) MATSUMOTO ET AL.	
	Examiner A. Sefer	Art Unit 2826	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *4-7 and 13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-3 and 8-12 in Paper No. 7 is acknowledged. The traversal is on the ground(s) that the species were not shown to be mutually exclusive and that searching the entire application would not place a serious burden on the examiner. This is not found persuasive because embodiments 1-8 are distinct. Hence, the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumura et al (JP 58-124243).

Matsumura et al disclose a semiconductor device having an SOI

structure including a semiconductor substrate, a buried insulating layer and an SOI layer, comprising: a MOS transistor provided in an element formation region of said SOI layer; and a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film 39 provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region 40 to be a part of said SOI layer present in a lower layer portion of said SOI layer, said MOS transistor including: source and drain regions 43, 44 of a first conductivity type selectively formed in said SOI layer, respectively, wherein said source and drain regions having such depths as to reach said buried insulating layer (as in claim 9); a gate electrode 41 having a gate electrode main part formed through a gate oxide film 42 on a region of said SOI layer between said source and drain regions; and a body region 45 having a body region main part to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion 46 electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential.

As to claim 8, Matsumura et al disclose a partial isolation film lower semiconductor region having a second conductivity type formed in contact with said body region, said semiconductor device further comprising an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

As to claim 10, Matsumura et al disclose source and drain regions having such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

4. Claims 1 and 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kunikiyo US Patent No. 6,429,505.

Kunikiyo discloses in figs. 27-29 and 31 a semiconductor device having an SOI structure including a semiconductor substrate 2, a buried insulating layer 3 and an SOI layer, comprising: a MOS transistor provided in an element formation region of said SOI layer; and a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film 81 provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region 89 to be a part of said SOI layer present in a lower layer portion of said SOI layer, said MOS transistor including: source and drain regions 83, 84 of a first conductivity type selectively formed in said SOI layer, respectively, wherein said source and drain regions having such depths as to reach said buried insulating layer (as in claim 9); a gate electrode 86 having a gate electrode main part formed through a gate oxide film 85 on a region of said SOI layer between said source and drain regions; and a body region 82 having a body region main part to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion 87 electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential.

As to claim 8, Kunikiyo discloses a partial isolation film lower semiconductor region having a second conductivity type formed in contact with said body region, said semiconductor device further comprising an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

As to claim 10, Kunikiyo discloses source and drain regions having such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

5. Claims 1-3 and 8-9 are rejected under 35 U.S.C. 102(a) as being anticipated by Maeda et al. (EP 1 115 158).

Maeda et al disclose in figs. 7 and 8 a semiconductor device having an SOI structure including a semiconductor substrate, a buried insulating layer 20 and an SOI layer 10, comprising: a MOS transistor provided in an element formation region of said SOI layer; and a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film 14 provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region 10b to be a part of said SOI layer present in a lower layer portion of said SOI layer, said MOS transistor including: source and drain regions 11, 12 of a first conductivity type selectively formed in said SOI layer, respectively, wherein having such depths as to reach said buried insulating layer (as in claim 9); a gate

electrode 151 having a gate electrode main part 15e formed through a gate oxide film 15d on a region of said SOI layer between said source and drain regions; and a body region having a body region main part 10a to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion 13 electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential.

As to claim 2, Maeda et al disclose said body region potential setting section includes a body region source/drain adjacent portion 10c in a gate width direction adjacently to said source and drain regions and extended in a gate length direction from said body region main part; and said gate electrode further has a gate extension region 15b extended in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, and serving to electrically block said body region source/drain adjacent portion and said source and drain regions through said gate extension region.

As to claim 3, Maeda et al disclose said body region source/drain adjacent portion includes a first body region source/drain adjacent portion extended in a first direction from said body region main part and a second body region source/drain adjacent portion extended in a second direction opposite to said first direction from said body region main part, and said gate extension region includes a first gate extension region formed on a vicinity of said first body region source/drain adjacent portion and a second gate extension region extended on a vicinity of said second body region source/drain adjacent portion.

As to claim 8, Maeda et al discloses a partial isolation film lower semiconductor region having a second conductivity type formed in contact with said body region, said semiconductor device further comprising an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

As to claim 10, Maeda et al discloses source and drain regions having such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

6. Claims 1 and 8-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Matsumoto et al. (JP 2000284599).

Matsumoto et al disclose in figs. 1 and 2 a semiconductor device having an SOI structure including a semiconductor substrate 1, a buried insulating layer 2 and an SOI layer 2, comprising: a MOS transistor provided in an element formation region of said SOI layer; and a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film 5b provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region 3b to be a part of said SOI layer present in a lower layer portion of said SOI layer, said MOS transistor including: source and drain regions 6 of a first conductivity type selectively formed in said SOI layer, respectively, wherein said source and drain regions having such depths as to reach said buried insulating layer (as

in claim 9); a gate electrode 156 having a gate electrode main part formed through a gate oxide film 15d on a region of said SOI layer between said source and drain regions; and a body region having a body region main part 3a to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion 3d electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential.

As to claim 8, Matsumoto et al disclose a partial isolation film lower semiconductor region having a second conductivity type formed in contact with said body region, said semiconductor device further comprising an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

As to claim 10, Matsumoto et al disclose source and drain regions having such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

As to claim 11, Matsumoto et al disclose in figs. 36-38 source and drain regions having such depths that said buried insulating layer is not reached and a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

As to claim 12, Matsumoto et al disclose in figs. 36-38 a drain region having a greater depth than a source region and has such a depth depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura et al. in view of Higashi et al. (EP 962988).

Matsumura et al do not disclose a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

Higashi et al disclose in fig. 1 source and drain regions 12 5 having such depths that said buried insulating layer is not reached and a depletion layer extended from said drain region reaches said buried insulating layer 2 during a normal operation.

Therefore it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Higashi et al with Matsumura et al, since that eliminate instability of operation due to fluctuation of potential.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura et al. in view of Higashi et al as applied to claims 1 and 11 above, and further in view of Redwine et al. US Patent No. 5,349,225.

The combined references fail to disclose a drain region having a greater depth than a source region.

Redwine et al disclose in fig. 8 a drain region having a greater depth than a source region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Redwine et al with the combined refrences above, since that would minmize the effect of hot carriers and impact ionization near the drain region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
September 20, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800